EE/CprE/SE 492 Status Report 5
March 13 – March 26

Group number: **22**

Project title: **ReRAM Compute ASIC Fabrication**

Client &/Advisor: **Cheng Wang & Henry Duwe**

Team Members/Role:

Ali Mannan
Tyler Kloser
Austin Miller
Vinicius Malaman Soares

- **Weekly Summary**
  - Organized all files necessary for a completed 1-bit design up to the layout stage
  - Analyzed configurations of crossbar with respect to matrix multiplication operations
  - All 1-bit components ready to be assembled
- **Past week accomplishments**
  - Vinicius Malaman Soares: Worked on finding designs for the ADC to work using the comparator and previous teams work.
  - Tyler Kloser: Continued with precheck and started creating a comprehensive guide for precheck, Brought over another teams mux designs and tried testing them.
  - Ali Mannan: Compiled files for the DAC, transimpedance amplifier, and ADC. All components have been tested and work as expected with and without parasitic extraction. Read some research papers with Austin on ReRAM crossbar design, and how to configure the components to achieve the goal of compute.
  - Austin Miller: Made good progress on setup script, should allow for easy and uniform setup for final completion and later groups/chipforge members. Experimented a bit more with reram in magic, still not as straightforward as I would like.
- **Pending issues**
  - Tyler Kloser: N/A
  - Ali Mannan: N/A
  - Austin Miller: Script needs a couple of small changes (PATH update, auto docker install, moving rc files to respective folders). Reram sometimes brings what looks like more pins than expected if generating from spice file in magic.
  - Vinicius Malaman Soares: N/A

- **Individual contributions**

NAME	Individual Contributions	Hours this period	HOURS cumulative
Tyler Kloser	Precheck and mux work	6	31
Ali Mannan	Testing of DAC, ADC, and transimpedance amplifier as an op-amp and a comparator. Shortlisted compute architectures	12	57
Austin Miller	Universal script nearly complete, some more reram layout experimentation	8	56
Vinicius Malaman Soares	ADC schematic design for higher bit crossbar	5	30

- **Comments and extended discussion**
    - N/A

Plans for the upcoming week

- Ali Mannan: Test a fully assembled 1-bit design, and possibly create other designs leveraging different compute architectures.
- Tyler Kloser: Start checking all components through precheck, maybe test the 1-bit design
- Austin Miller: Investigate how we'll get our different forming, setting, and resetting voltages to our desired cells and possible pulse generation. Finalize setup script. Knowledge dump into our MS Teams team posts.
- Vinicius Malaman Soares: Will work more on finding ADC designs and find an ADC that meets our requirements

- **Summary of weekly advisor meeting**
    - Provided a summary of current progress
    - Discussed in detail what went wrong with previous ReRAM submissions, and the steps we may take to avoid facing the same issues (identified the component that caused the issue but not the exact reason)
    - Discussed the viability of using an inverter as an ADC for a 1-bit design. Client suggested using a comparator
    - Client made it known that the final product having different sized ReRAM modules is not a priority